Research Laboratories No. 67-9F1-SCFAB-R1

January 1967

DESIGN AND FABRICATION OF AN ANALOG VOLTAGE TO DUTY CYCLE GENERATOR

THIRD INTERIM PROGRESS REPORT

Contract No. NAS7-100
Task Order Number RD-28

JPL No. 951306

Prepared for

California Institute of Technology
Jet Propulsion Laboratory
4800 Oak Grove Drive
Pasadena, California

by

Westinghouse Research Laboratories
Beulah Road
Pittsburgh, Pennsylvania 15235

Approved:

DESIGN AND FABRICATION OF AN ANALOG VOLTAGE TO DUTY CYCLE GENERATOR

THIRD INTERIM PROGRESS REPORT

Contract No. NAS7-100
Task Order Number RD-28

Prepared for

California Institute of Technology
Jet Propulsion Laboratory
4800 Oak Grove Drive
Pasadena, California

by

Westinghouse Research Laboratories
Beulah Road
Pittsburgh, Pennsylvania 15235

This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, sponsored by the National Aeronautics and Space Administration under Contract NAS7-100.

SUMMARY

Previous work on this project was carried out by the Westinghouse Molecular Electronics Division. It was decided in September 1966 to transfer the project to the Westinghouse Research Laboratories. This report covers the period from October to December 1966 during which the background information and prototype models were recieved by the Research Laboratories and a course of familiarization with the problems involved was carried out.

A review of the current design indicates that it may be possible to reduce the size of the integrating capacitor from 0.05 Mfd to 0.0005 Mfd without degradation of linearity. This will greatly reduce the fabrication problems for the capacitor.

INTRODUCTION

The requirement for the project is in integrated circuit form, of a circuit which converts a variable low power level, dc signal to a digital output such that the digital output 'on' time portion of the cycle is proportional to the dc input signal.

The original decision was to adopt a combined digital-analog approach and to utilize tantalum capacitors and also tantalum resistors for those components requiring close ratio control. The system can be divided into eight parts as shown in the schematic of Figure 1.

Two major areas of work were being undertaken:
(a) to bring the system into a suitable configuration for complete integration utilizing Westinghouse WS 177 "Instacircuits" as an intermediate stage, and (b) to develop the necessary associated tantalum capacitors and precision resistors.

The systems design had reached the point where the entire system had been breadboarded utilizing ten instacircuits but with some external components. The layout designs for complete integration have not yet been carried out although some consideration as to the required chip size and packaging had been given.

The tantalum component work had reached the stage where a reasonable yield of large capacitors could be achieved utilizing aluminum counter electrodes. Stability of the counter electrodes had not been investigated.

The majority of the effort in the present period was taken up by the problems of transfer of background information and familiarization with the operation of the "instacircuit" breadboard. Some re-evaluation of the

circuit design was also carried out with particular emphasis to those areas which would ease the fabrication problems such as reductions of capacitor size or relaxation of component tolerances.

DESIGN CONSIDERATIONS

The first working breadboard model of the AVDC Generator was studied partly for familiarization purposes and partly for design review. Overconservative design of the timing and comparison waveform generator seems apparent, and linearity measurements show that the integrating capacitor may be reduced for the 0.05 Mfd value of the original design to 0.0005 Mfd with no degradation of linearity. These measurements made at room temperature and at 2.5 kc basic operating frequency are to be repeated at low and high temperatures. Use of a smaller integrating capacitor will alleviate the capacitor fabrication problem and will permit use of a simpler integrator drive circuit. The study also showed that since the duty cycle output of the generator is independent of slope-symmetry of the timing and comparison waveform, the integrating operational amplifier need not have the high dc stability which the differential pin design affords and should be replaceable by a single-ended amplifier having only half as many components. Alternative designs for the integrator driver and the operational amplifier which take advantage of these facts have been designed, breadboard versions of these have been constructed, and the new circuits are now ready for substitutional testing.

EVALUATION OF INSTACIRCUIT BREADBOARD

The overall linearity of the system was measured using the breadboard containing standard transistors and components. The measurement was made through the use of the time delay base of an oscilloscope. The linearity

of the delay was first checked with a time mark generator and found to be accurate to .02%. This data is shown in Figure 2. The test setup described above is capable of measuring any portion of the duty cycle generator output to an accuracy of .05%.

Linearity measurements on the overall system were made for two different conditions, namely, the condition for which the integrating capacitor of the operational amplifier is .05 μf and the condition for which this capacitor is changed to .0005 μf. The resistance associated with the integrating time constant was changed in accordance with the capacitor to maintain the same time constant. The input differential voltage variation was provided by the circuit arrangement shown in Figure 3. Potentiometer R_1 was adjusted to maintain a voltage spread over potentiometer R_2 of 100 mv. With R_2 set at its midpoint, potentiometer R_3 was then adjusted to balance out the differential amplifier. The voltage readings taken at the input of the differential amplifier during the linearity measurement were measured to an accuracy of .02%.

The results of this linearity measurement are shown in Figure 4. The upper curve, showing the larger deviation, corresponds to the system using the .05 μf capacitor. The lower curve, which shows the smaller deviation, corresponds to the system using the .0005 μf capacitor.

PLANS FOR THE NEXT REPORTING PERIOD

The evaluation of the discrete component breadboard will be continued and the instacircuit breadboard will also be evaluated. Linearity measurements will be repeated at 125°C. A number of new circuits will be tried in the operational amplifier in an attempt to reduce the number of

transistors. Preliminary layout design for silicon integrated components will be started. Once the required size for the tantalum components have been established the layout design for these will also be commenced.

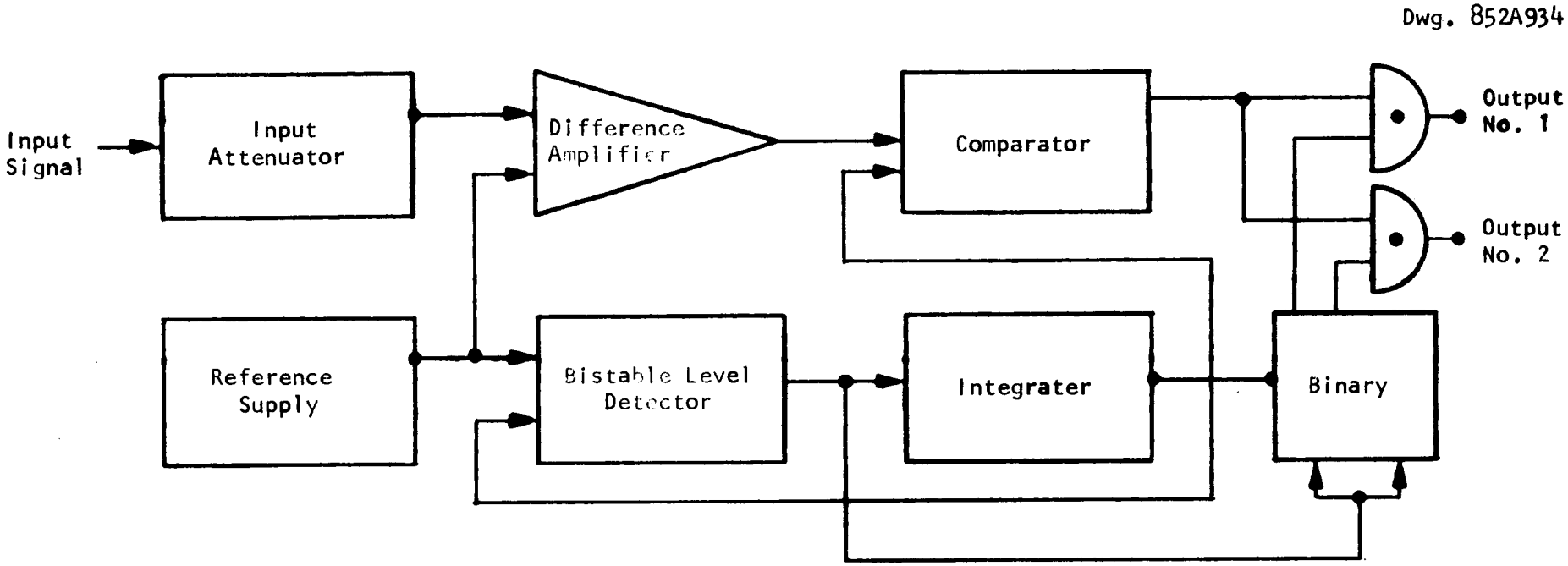

Fig. 1—Analog system block diagram

Calibration of 545 Tektronix Scope
Tektronix 180 Time Mark Generator

Time Mark (μSec)	Delay Multiplier Reading
0	000.0
10	050.5
20	100.8
30	150.5
40	200.5
50	250.6
60	300.8
70	350.6
80	400.7
90	450.2
100	500.2
110	550.0
120	599.7
130	649.5
140	699.2
150	749.0
160	798.9
170	848.6
180	898.3
190	947.9
200	997.8

Figure 2

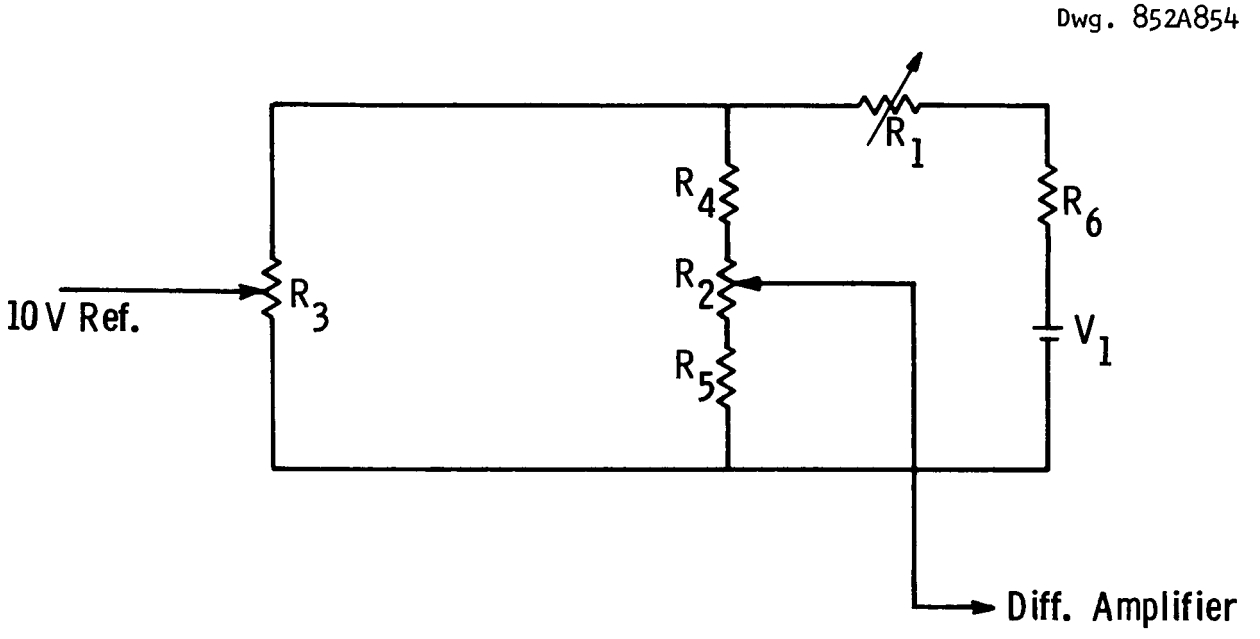

Fig. 3—Circuit to vary input voltage

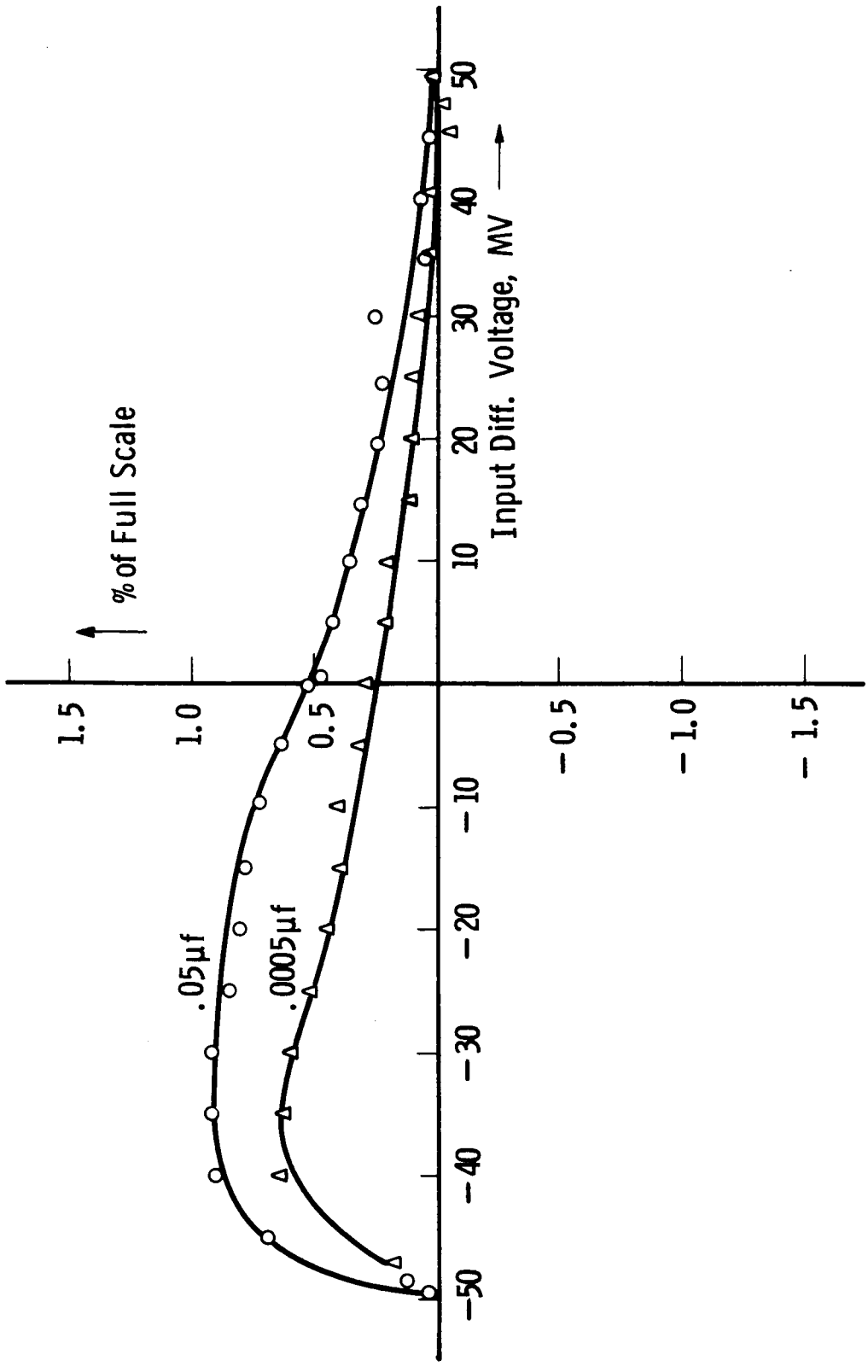

Fig. 4—Analog voltage to duty cycle generator system linearity

APPENDIX A

Data Log for

Discrete Component Breadboard

DISCRETE COMPONENT BREADBOARD

Results of Data Taken with .0005 μf
Capacitor and 100 K Resistance at 25°C

Read	Calc.	Meas.	Dev.	Inf. Diff.	%(FS)
975	0.00	0.0	0.00	.04715	0.00
970	4.89	5.7	- .81		- 0.08
965	9.79	11.0	- 1.21		- 0.12
960	14.69	15.4	- .71		- 0.07
950	24.48	19.5	4.98	.04479	0.50
900	73.46	73.70	0.06	.03974	0.01
850	122.43	122.3	0.10	.03476	0.01
800	171.40	171.0	0.40	.02973	0.04
750	220.38	219.6	0.78	.02482	0.08
700	269.35	268.4	0.95	.01977	0.10
650	318.33	317.4	0.93	.01481	0.09
600	367.30	365.4	1.90	.00998	0.19
550	416.27	414.2	2.00	.00500	0.20
500	465.25	462.4	2.85	.00000	0.29
450	514.22	511.1	3.12	.00505	0.31
400	563.20	559.2	4.00	.00985	0.40
350	612.17	608.1	4.07	.01502	0.41
300	661.14	656.6	4.54	.01980	0.45
250	710.12	705.1	5.02	.02490	0.50
200	759. 09	753.2	5.89	.02988	0.59
150	808.07	802.0	6.07	.03492	0.61
100	857.04	851.0	6.04	.03991	0.60
0	954.99	955.0	0.00	.04976	0.00
50	906.00	906.8	- .80	.04487	- 0.08
30	925.60	923.8	+ 1.80		- 0.18

DISCRETE COMPOUND BREADBOARD

Results of Data Taken with .05 μf Capacitor and 1 K Resistance at 25°C

Read	Calc.	Meas.	Dev.	Inf. Diff.	%(FS)
975	00.00	00.0	0.00	.04715	.0
950	24.58	24.4	0.18	.04479	.02
900	73.70	73.1	0.60	.03974	.06
850	122.90	122.5	0.40	.03476	.04
800	172.12	170.7	2.50	.02973	.25
750	221.30	219.2	2.10	.02482	.21
700	270.48	268.0	2.48	.01977	.25
650	319.66	316.5	3.16	.01481	.32
600	368.84	365.3	3.54	.00998	.35
550	418.02	413.8	4.22	.00500	.42
500	467.20	461.4	5.20	.00000	.52
450	516.37	510.0	6.37	.005050	.64
400	565.55	558.6	7.15	.009850	.72
350	614.75	607.0	7.75	.015020	.78
300	663.90	655.8	8.10	.019800	.81
250	713.09	704.5	8.50	.02490	.85
200	762.27	753.0	9.27	.02988	.93
150	811.45	802.2	9.25	.03492	.93
100	860.63	851.5	9.13	.03991	.91
50	909.81	902.8	7.01	.04487	.70
25	934.40	933.5	0.90	.04840	.09
5	954.07	954.2	+ 0.05	.04938	.01
0	959.90	959.9	0.00	.04976	.00

Linearity Calibrator of Discrete Component Breadboard
Time Constant: 1.2 KΩ and .005 μf in parallel with
.003 μF; Time base 20 μsec/division

Input Voltage Dial	Delay Time Dial (0-200 μsec FS)
0000	
0000	951.5
0050	886.8
0100	812.7
0150	742.2
0200	671.5
0250	600.7
0300	529.9
0350	458.7
0400	388.1
0450	318.2
0500	245.7
0550	175.3
0600	105.0
0650	036.3
0700	

Linearity Calibration of Discrete Component Breadboard

Input Voltage	Dial	Delay Time Dial
975.0	.00283	0010.0
950.0	.00519	034.4
900.0	.01024	083.1
850.0	.01522	132.5
800.0	.02025	180.7
750.0	.02516	229.2
700.0	.03021	278.0
650.0	.03517	326.5
600.0	.04010	375.3
550.0	.04497	423.8
500.0	.04998	471.4
450.0	.05503	520.0
400.0	.05993	568.6
350.0	.06500	617.0
300.0	.06988	665.8
250.0	.07488	714.5
200.0	.07986	763.0
150.0	.08490	812.2
100.0	.08989	861.5
050.0	.09485	912.8
025.0	.09838	943.5
005.0	.09936	968.2
000.0	.09974	969.9
Additional Points		
775.0	.00282	0010.1
970.0	.00335	0016.6
965.0	.00384	0022.0
960.0	.00434	0026.2
955.0	.00477	0030.7
945.0	.00582	0040.2

Voltage Meas. with Beckman No. 4910 DVM .002% FS Lin., Res. .005% FS, Stabil. 101% FS/Year.

Pot. voltage is .09996 V with Pot. set midscale.

Calibration of Discrete Component Breadboard
Time Constant: .0005 μF with 100 KΩ

Input Voltage Dial	Delay Time Dial
975.0	0010.1
970.0	0015.7
965.0	0021.0
960.0	0025.4
950.0	0029.5
900.0	0083.7
850.0	00132.3
800.0	0181.0
750.0	0229.6
700.0	0278.4
650.0	0327.4
600.0	0375.4
550.0	0424.2
500.0	0472.4
450.0	0521.1
400.0	0569.2
350.0	0618.1
300.0	0666.6
250.0	0715.1
200.0	0763.2
150.0	0812.0
100.0	0861.0
000.0	0965.0
Additional Points	
0010.0	0960.0
0015.0	0956.0
0020.0	0949.4
0025.0	0941.2
0030.0	0933.8
0035.0	0928.3
0040.0	0923.4
0045.0	0916.8